Notice of References Cited	Application/Control No. 10/092,328	Applicant(s)/Patent Under Reexamination CARLSON, DAVID A.	
	Examiner David G. Cervetti	Art Unit 2136	Page 1 of 4

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,873,707	03-2005	Batcher, Kenneth W.	380/255
	B	US-6,549,622	04-2003	Matthews, Jr., Donald P.	380/29
	C	US-6,369,813	04-2002	Pentkovski et al.	345/419
	D	US-6,356,270	03-2002	Pentkovski et al.	345/530
	E	US-6,643,745	11-2003	Palanca et al.	711/138
	F	US-6,223,276	04-2001	Lee et al.	712/207
	G	US-2002/0004904	01-2002	Blaker et al.	713/190
	H	US-6,704,871	03-2004	Kaplan et al.	713/192
	I	US-6,421,730	07-2002	Narad et al.	709/236
	J	US-5,454,117	09-1995	Puziol et al.	712/23
	K	US-5,799,165	08-1998	Favor et al.	712/214
	L	US-5,754,812	05-1998	Favor et al.	712/216
	M	US-5,926,642	07-1999	Favor, John G.	712/1

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Bruce Schneier, Doug Whiting, Fast Software Encryption: Designing Encryption Algorithms for Optimal Software Speed on the Intel Pentium Processor, Lecture Notes in Computer Science, Volume 1267, Jan 1997, Page 242
	V	Mosanya et al., CryptoBooster: A Reconfigurable and Modular Cryptographic Coprocessor, 1999, Springer Verlag Berlin, pp 246-256.
	W	Wollinger et al., How Well Are High-End DSPs Suited for the AES Algorithms?, April 2000, Texas Instrument.
	X	Shehata et al., VLSI Implementation of a High Speed Block-Cipher Module, 2001, IEEE.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 10/092,328	Applicant(s)/Patent Under Reexamination CARLSON, DAVID A.	
	Examiner David G. Cervetti	Art Unit 2136	Page 2 of 4

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chodowiec et al., Fast implementations of secret-key block ciphers using mixed inner- and outer-round pipelining, February 2001, ACM.
	V	Hong et al., Hardware Design and Performance Extimation of the 128-bit Block Cipher CRYPTON, 1999, Springer-Verlag Berlin, pp 49-60.
	W	McLoone et al., Single-Chip FPGA Implementation of the Advanced Encryption Standard Algorithm, 2001, Springer-Verlag Berlin, pp 152-161.
	X	Moldovyan et al., A Cipher Based on Data-Dependent Permutations, August 2001, Journal of Cryptology, pp 61-72.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 10/092,328	Applicant(s)/Patent Under Reexamination CARLSON, DAVID A.	
	Examiner David G. Cervetti	Art Unit 2136	Page 3 of 4

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lin et al., A VLSI Implementation of the Blowfish Encryption/Decryption Algorithm, 2000, IEEE.
	V	Childers et al., Architectural Considerations for Application-Specific Counterflow Pipelines, March 1999, IEEE, Advanced Research in VLSI.
	W	Sherigar et al., A pipelined parallel processor to implement MD4 message digest algorithm on Xilinx FPGA, January 1998, IEEE, Eleventh International Conference on VLSI Design, pp 394-399.
	X	Craig Clapp, Optimizing a Fast Stream Cipher for VLIW, SIMD, and Superscalar Processors, 1997, Proceedings of Fast Software Encryption Workshop.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 10/092,328	Applicant(s)/Patent Under Reexamination CARLSON, DAVID A.	
	Examiner David G. Cervetti	Art Unit 2136	Page 4 of 4

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Ye et al., CHIMAERA: a high-performance architecture with a tightly-coupled reconfigurable functional unit, 2000, IEEE, Proceedings of the 27th International Symposium on Computer Architecture, pp 225-235.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.